**Lab # 08**

**8-bit Ring Counter On Seven Segment Display**

CSE-308L [DIGITAL SYSTEM DESIGN LAB](https://classroom.google.com/c/NTk1NjYyOTEyNzU5)

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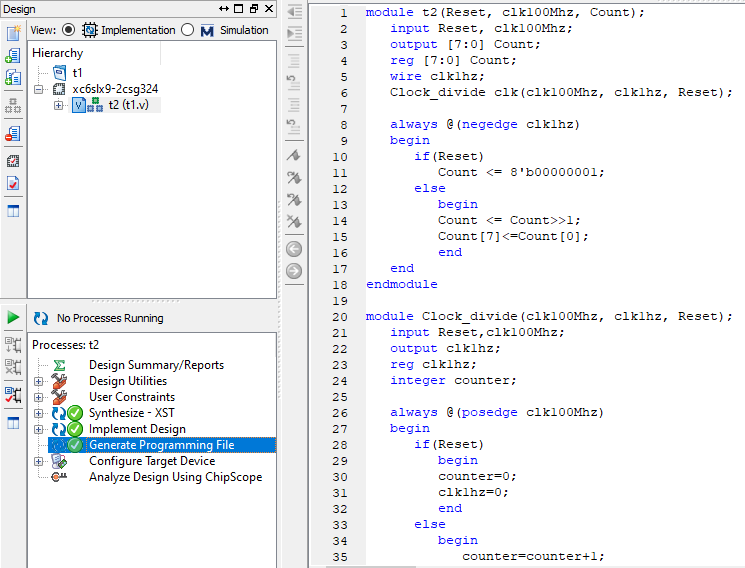
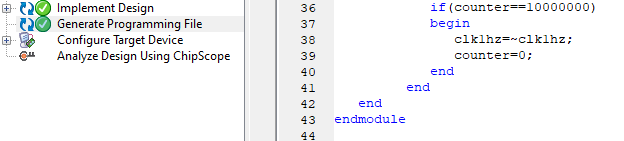
**Objective**

To Implement an 8 Bit Ring Counter on Spartan 3 FPGA starter kit to show its output on the seven-segment display.

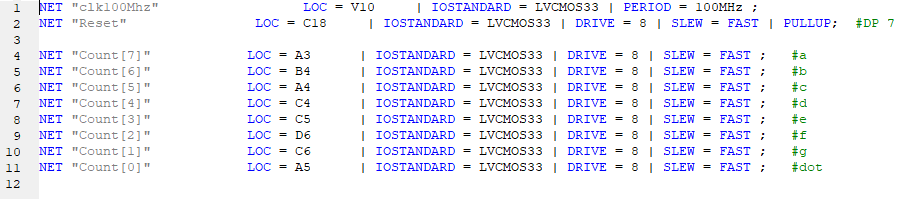
**Lab Task**

Implement an 8-bit ring counter on the seven-segment display.

**Code**

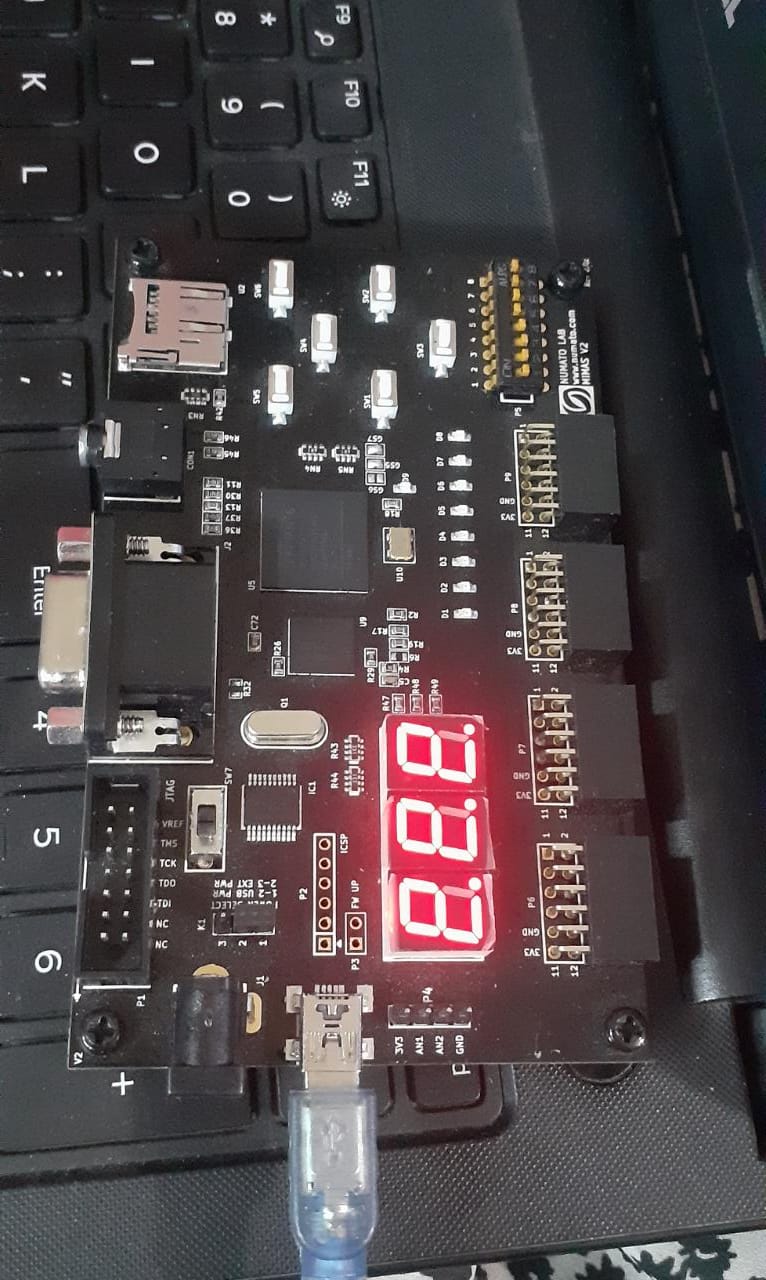
 

**User Constraint File(ucf)**



**Output**

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